**Lab Report 1**

Answers to questions from 1.b:

In the diagram area, (1) is the constant cA which is set to 5 on line 50. For this specific instance of the quadratic module, cA is connected to the input iA (line 44) of g\_Mult1.

In the diagram area, (2) is the iX defined as an integer on line 26. For this specific instance of the quadratic module, iX is fed into iB (line 45) of g\_Mult1.

In the diagram area, (3) is the constant cB which is set to 23 on line 51. For this specific instance of the quadratic module, cB is connected to the input iA of g\_Mult2.

In the diagram area, (4) is the constant cC which is set to 2 on line 52. For this specific instance of the quadratic module, cC is connected to the input iB (line 38) of g\_Add1.

In the diagram area, (5) the clock iCLK is defined on line 25 as std\_logic.

In the diagram area, (6) iA is an integer which is defined on line 44. For this specific instance of the quadratic module, iA is implemented on line 69 and is set to cA in g\_Mult1.

In the diagram area, (7) iB is an integer which is defined on line 45. For this specific instance of the quadratic module, iB is implemented on line 70 and is set to iX in g\_Mult1.

In the diagram area, (8) is just a simple multiplier symbol to show that iA and iB are being multiplied.

In the diagram area, (9) is just a simple symbol to show that on a positive clock edge, the two values will get multiplied.

In the diagram area, (10) oC is an integer which is defined on line 46. For this specific instance of the quadratic module, oC is implemented on line 71 and is set to signal sVALUE\_Ax in g\_Mult1.

In the diagram area, (11) g\_Mult1 is the first multiplier of the circuit. It is defined on Line 67 and holds the values of iCLK, iA, iB and oC.

In the diagram area, (12) iA is an integer which is defined on line 44. For this specific instance of the quadratic module, iA is implemented on line 76 and is set to cB in g\_Mult2.

In the diagram area, (13) iB is an integer which is defined on line 45. For this specific instance of the quadratic module, iB is implemented on line 77 and is set to iX in g\_Mult2.

In the diagram area, (14) oC is an integer which is defined on line 46. For this specific instance of the quadratic module, oC is implemented on line 78 and is set to signal sVALUE\_Bx in g\_Mult2.

In the diagram area, (15) g\_Mult2 is the first multiplier of the circuit. It is defined on Line 74 and holds the values of iCLK, iA, iB and oC.

In the diagram area, (16) iA is an integer defined on line 37. For this specific instance of the quadratic module, iA is implemented on Line 91 and is set to sVALUE\_Bx in g\_Adder1.

In the diagram area, (17) iB is an integer defined on line 38. For this specific instance of the quadratic module, iB is implemented on Line 92 and is set to cC in g\_Adder1.

In the diagram area, (18) is just a simple symbol to show that iA and iB are being added together.

In the diagram area, (18) is just a simple symbol to show that iA and iB are being added together.

In the diagram area, (19) is just a simple symbol to show that on a positive clock edge, iA and iB are being added together.

In the diagram area, (20) oC is an integer which is defined on line 39. For this specific instance of the quadratic module, oC is implemented on line 93 and is set to signal sVALUE\_BxpC in g\_Add1.

In the diagram area, (21) iA is an integer which is defined on line 44. For this specific instance of the quadratic module, iA is implemented on line 85 and is set to sVALUE\_Ax in g\_Mult3.

In the diagram area, (22) iB is an integer which is defined on line 45. For this specific instance of the quadratic module, iB is implemented on line 86 and is set to iX in g\_Mult3.

In the diagram area, (23) oC is an integer which is defined on line 46. For this specific instance of the quadratic module, oC is implemented on line 87 and is set to signal sVALUE\_Axx in g\_Mult3.

In the diagram area, (24) g\_Mult3 is the third multiplier of the circuit. It is defined on Line 83 and holds the values of iCLK, iA, iB and oC.

In the diagram area, (25) iA is an integer which is defined on line 44. For this specific instance of the quadratic module, iA is implemented on line 100 and is set to sVALUE\_Axx in g\_Add2.

In the diagram area, (26) iB is an integer which is defined on line 45. For this specific instance of the quadratic module, iB is implemented on line 101 and is set to sVALUE\_BxpC in g\_Add2.

In the diagram area, (27) oC is an integer which is defined on line 46. For this specific instance of the quadratic module, oC is implemented on line 102 and is set to signal oY in g\_Add2.

In the diagram area, (28) g\_Add2 is the second adder of the circuit. It is defined on Line 98 and holds the values of iCLK, iA, iB and oC.

In the diagram area, (29) oY is the final output of the circuit. It is defined on Line 27 and holds the values of the quadratic equation –

In the diagram area, (30) g\_Add2 is the second adder of the circuit. It is defined on Line 89 and holds the values of iCLK, iA, iB and oC.

1h)

The timing waveform is wound together to the adder. Whenever the there is a positive clock edge, the values get added step by step. On a negative clock edge, the values always stay the same. Once we get to the output of the second adder, there will be no more changes so we get the final output of the equation. It takes a total of three clock cycles to get to the final output.